SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]
CIT Campus, MGR Knowledge City, Taramani, Chennai–600113, India

Advertisement No. SETS/Chn/Rec/Proj/2025-26/44 Date: 21st October 2025

Society for Electronic Transactions and Security [SETS] is a Society under the Societies Registration Act, XXI of 1860, dedicated to carry-out Research and Development in the field of Information Security focusing on the key verticals, namely, Cryptology and Computing, Hardware Security, Quantum Security and Network Security.

SETS invites applications from citizens of India to fill up the following positions for a Research & Development project in the area of Cybersecurity:

The descriptions of position, detailed qualification requirements and salary are given below:

Name of Post	**Project Associate**
Total Number of Posts	FIVE
Age Limit	Not more than 35 years as of closing date of advertisement
Experience	0-2 Years of Relevant Experience
Remuneration	Consolidated salary would be Rs. 40,000/- to 60,000/- per month based on the higher qualification and relevant experience

Domain	**Software Post Code: 25-PAS-14**
No. of posts for the domain	THREE
Essential Qualification	First Class B. Tech /B. E in Computer Science / Information Technology/ Information Security/ Cyber Security / ECE or equivalent
Desirable Qualification	First Class M. Tech / M.E in Computer Science / Information Technology/ Information Security/ Cyber Security or equivalent
Areas of Skill sets/ Knowledge required	a) Programming Experience in C/C++, Python and MATLAB. b) Experience in Software testing (manual and/or automation). c) Knowledge of Linux/windows Operating System. d) Knowledge in Cryptography & Cybersecurity. e) Knowledge in Hardware Security/ Side Channel Analysis. f) Knowledge in Digital Electronics. g) Hands-on Experience in Penetration Testing Tools, Web Application Security and Linux Hardening.

	h) Knowledge on RTOS based firmware. i) Experience in Exploit Development, code reverse engineering., binary analysis tools (E.g. Ghidra, IDA Pro), Assembly language for ARM, MIPS and x86 architectures. j) Problem-Solving, Analytical Thinking capabilities.

Domain	**Hardware Post Code: 25-PAH-15**
No. of posts for the domain	TWO
Essential Qualification	First Class M. Tech /M. E in VLSI Design /Embedded Systems/ Electronics & Communication/ Communication Systems /Applied Electronics/ Computer Science or equivalent
Areasof Skill sets / Knowledge required	a) FPGA Realization with VHDL/Verilog & Xilinx Vivado Tools b) Programming Experience in C/C++, Python and MATLAB. c) Knowledge in signal processing and experience with MATLAB and the System Generator tool of Vivado d) Expertise in Hardware Security & Side-Channel Analysis e) Knowledge in Digital Electronics f) Knowledge of hardware components like Processors, Memory, Peripherals and storage device g) Knowledge of various communication protocols for interfacing between devices h) Knowledge of circuits and PCB. i) Hands-on experience in Hardware debugging tools j) Knowledge of Linux and Windows Operating Systems k) Problem-Solving, Analytical Thinking capabilities.

The positions of **Project Associate** as proposed is purely temporary and would be filled on a contract basis with a consolidated salary under project mode. The duration of the assignment is initially for a period of One Year and would be extended further based on the need of the project and performance. There is no scope of continuation / regularization/ absorption under any circumstances.

Application Procedure:

Name of the Post	Domain	Post Code
Project Associate	Software	25-PAS-14
Project Associate	Hardware	25-PAH-15

1. Candidates are requested to provide the following details & Supporting documents: -
    a) Enter all required details in the form given in **www.setsindia.in/careers** and submit. Applications lacking required details, such as experience certificate, Proof of academic qualification, contact details will be rejected.
    b) Scanned copies of academic certificates (Single PDF document)
    c) Scanned copies of Experience certificates (Single PDF document)
2. The last date for uploading applications is 07.11.2025 before 6 PM.
3. Shortlisted candidates would be required to attend a Written Test and / or Interview at SETS, Chennai. The date and time for this would be intimated to shortlisted candidates by E-mail.

Terms and Conditions:

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the interview day.
2. No TA/DA will be given to candidates appearing for interview.
3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.
4. Number of vacancies may increase/decrease depending upon SETS requirements and such changes will be made by SETS without any notice.

Executive Director