



Strategy and Synergy for Security



SETS & C-DAC Jointly Offers Workshop on **SECURE PROCESSOR 2026**

**Date & Time: March 2nd - 3rd,
2026 & 9:30AM - 6PM**

**Location: SETS, MGR Film City
Road, CIT Campus, Taramani,
Chennai, Tamil Nadu 600113**

WORKSHOP OVERVIEW

This workshop offers a forward-looking introduction to security considerations in modern processor design. It explores how trust is established at the hardware level and how architectural choices influence long-term system security. Participants will explore evolving threat landscapes, including physical, side-channel, and supply-chain attacks, alongside future-ready defensive design strategies.

HIGHLIGHTS OF THE WORKSHOP

- **Architecture Fundamentals:** Security-conscious processor design based on core computer architecture principles.
- **Hardware Root of Trust:** On-chip identity, secure key storage, and reliable entropy generation.
- **Cryptographic Integration:** PUF- and TRNG-based hardware mechanisms for unique device identity.
- **Lightweight Secure Boot:** Efficient chain-of-trust boot for resource-constrained systems using cryptographic primitives
- **Secure Boot Standards:** Secure boot aligned with NIST SP 800-193 and PSA concepts.
- **Remote Attestation:** Cryptographic proof of firmware integrity to a remote verifier.
- **Advanced Defence Mechanisms:** Protection against side-channel attacks and physical tampering.
- **Trusted Execution:** Secure isolation using Trusted Execution Environments (TEEs).
- **Open Architectures (RISC-V):** Security opportunities, risks, and trade-offs in open architectures.
- **Hands-on Demos:** Live root-of-trust & secure-boot demonstrations.

CHIEF GUESTS

Context Setting by: **Shri. Manoj Jain**, MeitY

Chief Guest Address: **Shri. E. Magesh**, Director General, C-DAC.

DOMAIN EXPERTS

1. **Prof. Santanu Sarkar**, IIT Madras
 2. **Prof. Chester Rebeiro**, IIT Madras
 3. **Prof. Debapriya Basu Roy**, IIT Kanpur
 4. **Prof. Debayan Das**, IISc Bengaluru
 5. **Mr Libin T T**, C-DAC Trivandrum
 6. **Ms Sajna V P**, C-DAC Trivandrum
 7. **Ms Jaya S**, C-DAC Trivandrum
 8. **Dr Natarajan**, SETS Chennai
 9. **Dr Tapabrata Roy**, SETS Chennai
 10. **Dr Vishal Saraswat**, Bosch Global Software Technologies Pvt Ltd.
 11. **Mr Madhusudan**, Incore Semiconductor Pvt Ltd.
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REGISTRATION

- **Fee:** Free of Cost.
 - **Capacity:** 40 Slots (First Come, First Serve).
 - **Registration Link:** <https://forms.gle/CQpSJ9npouU3AnkcQ7>.
 - **Mode of Attendance:** OFFLINE
 - **Target Audience:** Scholars, Researchers, Academia, and Industry professionals.
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PROGRAM COORDINATORS

- Dr Prem Laxman Das, Scientist, SETS, Chennai.
 - Dr Natarajan, Scientist, SETS, Chennai.
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CONTACT INFORMATION

For any queries or requests, kindly send an email to: qsrq_riscv@setsindia.net or reach out to the below contacts:

☎ Mr Raja Adhithan: +91 73391 98134

☎ Mr Sheik Abdullah: +91 97153 10341

Event Schedule (Tentative)

02/03/2026

9:30 - 10:30 AM

Inauguration

10:30 - 11:00 AM

High Tea

11:00 - 12:00 PM

Secure processor and its industrial application

Dr Vishal Saraswat

12:00 - 01:00 PM

Lightweight Cryptography

Dr Tapabrata Roy

01:00 - 02:00 PM

Lunch

02:00 - 03:00 PM

Overview of a secure processor and its application

Prof. Chester Rebeiro

03:00 - 04:00 PM

Overview of Vega Processor and its application

Mr Libin T T & Ms Sajna V P

04:00 - 04:30 PM

High Tea

04:30 - 05:30 PM

**Secure Boot Architecture for Indigenous Vega
Processor Based Systems - Ms Jaya S**

05:30 - 6:00 PM

C-DAC Demo

03/03/2026

9:30 - 10:30 AM

TBD
Prof. Debapriya Basu Roy

10:30 - 10:50 AM

High Tea

10:50 - 11:50 PM

**Hard Problems in Cryptography: From
Factorization to Post Quantum** - Prof. Santanu

11:50 - 12:50 PM

SCA-resilient PQ-secure processor design
Prof. Debayan Das

12:50 - 1:40 PM

Lunch

1:40 - 2:40 PM

TBD
Mr Madhusudan

2:40 - 3:40 PM

Remote Attestation
Dr Natarajan

3:40 - 4:00 PM

High Tea

4:00 - 4:45 PM

PUF & TRNG for Secure processor
Mr Raja Adhithan

4:45 - 5:30 PM

Secure Boot and its Standards
Mr Sheik Abdullah

5:30 - 6:00 PM

SETS Demo