SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]
CIT Campus, MGR Knowledge City, Taramani, Chennai–600113, India

Advertisement No. SETS/Chn/Rec/Proj/2026-27/63 Date: 18th August 2026

Society for Electronic Transactions and Security [SETS] is a Society under the Societies Registration Act, XXI of 1860, dedicated to carry-out Research and Development in the field of Information Security focusing on the key verticals, namely, Cryptology and Computing, Hardware Security, Quantum Security and Network Security.

SETS invites applications from citizens of India to fill up the following positions for a Research & Development project in the area of Cybersecurity:

1. **Project Scientist – 1 Position**
2. **Project Associate – 1 Position**

The descriptions of position, detailed qualification requirements and salary are given below:

1. Project Scientist

Name of Post	**Project Scientist Post Code: 26-PS-07**
Total Number of Posts	One
Age Limit	Not more than 40 years as on 27.08.2026
Essential Qualification	PhD in Science/ Statistics/ Mathematics/ Computer Science or M.E./M.Tech. /M.S. in Electrical /Electronics /Communication / VLSI Design/ Computer Science /Information Security/Quantum Computing/Quantum Technology (or) Equivalent with 60 % or above marks
Desirable Qualification	PhD in relevant Engineering discipline / Technology with specialization in Quantum Computing /Quantum Information security /Quantum cryptography / Cryptography
Experience	3(Three) to 7(Seven) Years of relevant experience Doctorate in Engineering is equivalent to 4 years
Remuneration	Salary would be Rs 70,000 to 1,00,000 per month, additional increment may be considered based on the skill sets and relevant experience of candidate.
Areas of Skill sets/ Knowledge required	a) Should have a good knowledge of quantum mechanics in general and all aspects related to quantum communications in particular. b) Knowledge of error correction algorithms in classical and Quantum c) Programming: Qiskit, Verilog/VHDL, C++, MATLAB, Python d) Proficiency in quantum computing fundamentals, including qubits, gates, noise, and decoherence. e) Hands-on experience in FPGA programming over SoC architecture.

Name of Post	Project Associate Post Code: 26-PA-15
Total Number of Posts	One
Age Limit	Not more than 35 years as on 27.08.2026
Essential Qualification	B.Tech / B.E in Electronics & Communication/Applied Electronics/VLSI Design / Embedded Systems with 60% or above marks
Desirable Qualification	M.Tech / M.E in Electronics & Communication/Applied Electronics/VLSI Design / Embedded Systems / Quantum Technology with 60% or above marks
Experience	0-4 Years of relevant experience Master's in Engineering is equivalent to 2 years
Remuneration	Consolidated salary would be Rs 40,000/ to 60,000/- per month, additional increment may be given based on the skill sets and relevant experience of candidate.
Areas of Skill sets/ Knowledge required	a) Programming: Verilog/VHDL, C++, Python b) Knowledge of hardware components like Processors, Memory, peripherals, and storage devices c) Hands-on experience in FPGA programming over SoC architecture. d) Experience with AMD (Xilinx) FPGA families e) Cryptography & Security

The positions of **Project Scientist & Project Associate** as proposed is purely temporary and would be filled on a contract basis with a consolidated salary under project mode. The duration of the assignment is initially for a period of One Year and would be extended further based on the need of the project and performance. There is no scope of continuation / regularization/ absorption under any circumstances.

Application Procedure:

Name of the Post	Post Code
Project Scientist	26-PS-07
Project Associate	26-PA-15

1. Candidates are requested to provide the following details & Supporting documents: -
   a) Scanned copy of Personal Particulars Form (pdf format) duly filled and signed. The Personal Particulars Form (PPF) is available at SETS homepage **https://setsindia.in/careers**
   b) Scanned copies of academic certificates (Single PDF document)
   c) Scanned copies of Experience certificates (Single PDF document)

2. Candidates are requested to attach the required documents, application with incomplete PPF form and without required certificates/documents are liable to be rejected.
3. The last date for applying for the posts is ~~28.08.2026~~ **07.09.2026 before 6:00PM**.
4. Shortlisted candidates would be required to attend a Written Test and / or Interview at SETS, Chennai.
5. The date and time for this would be intimated to shortlisted candidates by E-mail

Terms and Conditions:

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the interview day.
2. No TA/DA will be given to candidates appearing for interview.
3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.
4. Number of vacancies may increase/decrease depending upon SETS requirements and such changes will be made by SETS without any notice.

Executive Director