



**SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]**  
CIT Campus, MGR Knowledge City, Taramani, Chennai-600113, India

**Advertisement No. SETS/Chn/Rec/Proj/2026-27/72 Date: 14<sup>th</sup> October 2026**

**Society for Electronic Transactions and Security [SETS]** is a Society under the Societies Registration Act, XXI of 1860, dedicated to carry-out Research and Development in the field of Information Security focusing on the key verticals, namely, Cryptology and Computing, Hardware Security, Quantum Security and Network Security.

SETS invites applications from citizens of India to fill up the following positions for a Research & Development project in the area of Cybersecurity:

**1. Project Associate – 1 Position**

The descriptions of position, detailed qualification requirements and salary are given below:

| Name of Post                               | Project Associate      Post Code: 26-PA-23                                                                                                                                                                                                                                                                                                |
|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Total Number of Posts                      | One                                                                                                                                                                                                                                                                                                                                       |
| Age Limit                                  | Not more than 35 as on 30.10.2026                                                                                                                                                                                                                                                                                                         |
| Essential Qualification                    | B. E / B. Tech in Electronics and Communication or equivalent with 60% or above marks                                                                                                                                                                                                                                                     |
| Desirable Qualification                    | M.Tech /M. E / MS by Research in Embedded Systems/Communication Systems/VLSI Design/ Applied Electronics or equivalent with 60% or above marks                                                                                                                                                                                            |
| Experience                                 | 0-4 Years of relevant experience<br>Master's In Engineering is equivalent to 2 years                                                                                                                                                                                                                                                      |
| Remuneration                               | Consolidated salary would be Rs 40,000/ to 50,000/- per month, additional increment may be given based on the skill sets and relevant experience of candidate.                                                                                                                                                                            |
| Areas of Skill sets/<br>Knowledge required | a) Hands-on experience in Xilinx Vivado tools, simulation using MATLAB / ModelSim and FPGA realization using VHDL/Verilog programming<br>b) Knowledge in FPGA debug tools such as ILA<br>c) Programming Experience in C/C++ and Python<br>d) Knowledge in Digital Electronics<br>e) Knowledge in Hardware Security/ Side Channel Analysis |

The positions of **Project Associate** as proposed is purely temporary and would be filled on a contract basis with a consolidated salary under project mode. The duration of the assignment is initially for a period of One Year and would be extended further based on the need of the project and performance. There is no scope of continuation / regularization/ absorption under any circumstances.



## Application Procedure:

| Name of the Post  | Post Code |
|-------------------|-----------|
| Project Associate | 26-PA-23  |

- Candidates are requested to provide the following details & Supporting documents: -
  - Scanned copy of Personal Particulars Form (pdf format) duly filled and signed. The Personal Particulars Form (PPF) is available at SETS homepage <https://setsindia.in/careers>
  - Scanned copies of academic certificates (Single PDF document)
  - Scanned copies of Experience certificates (Single PDF document)
- Candidates are requested to attach the required documents, application with incomplete PPF form and without required certificates/documents are liable to be rejected.
- The last date for uploading applications is 30.10.2026 before 6 PM.
- Shortlisted candidates would be required to attend a Written Test and / or Interview at SETS, Chennai. The date and time for this would be intimated to shortlisted candidates by E-mail.

## Terms and Conditions:

- The shortlisted candidates would be required to bring all their original testimonials for verification on the interview day.
- No TA/DA will be given to candidates appearing for interview.
- The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.
- Number of vacancies may increase/decrease depending upon SETS requirements and such changes will be made by SETS without any notice.

**Executive Director**